FERROELECTRIC MEMORY DEVICE AND CONTROL METHOD THEREOF

ABSTRACT

A ferroelectric random access memory device according to the present invention includes a pulse generator circuit capable of generating a pulse signal in response to an address transition. A chip enable buffer circuit activates a chip enable flag signal in response to a first transition of the pulse signal. A row selector circuit selects and drives one of the rows in response to the address. The row selector circuit also generates a flag signal indicating a selection of a plate line. A control circuit activates a plate control signal in response to the activation of a write enable signal, and deactivates the plate control signal in response to a second transition of the pulse signal. A plate line of a selected row is re-activated according to activation of the plate control signal and is deactivated according to deactivation of the plate control signal.